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Application/Control Number: 09/693,044

Art Unit: 2673

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on 12 September 2003. These drawings are acceptable.

Allowable Subject Matter

- 3. Claims 1, 2, 4, 5, 7, 8, 10 and 19-23 (renumbered as claims 1-12) are allowed.
- 4. The following is a statement of reasons for the indication of allowable subject matter: The present invention comprises an active-matrix liquid crystal display apparatus. The closest prior art, Takeda et al. (US 5,398,043), discloses an active-matrix substrate including a plurality of scanning electrode lines [Fig. 1, 1], a plurality of data electrode lines [Fig. 1, 2], pixel electrodes [Fig. 1, A] and switching elements [Fig. 1, 3], the pixel electrodes being respectively connected to intersections of the plurality of scanning electrode lines and the plurality of data electrode lines via the switching elements; a counter electrode substrate including a counter electrode formed thereon, the counter electrode being opposed to the pixel electrodes; a liquid crystal [Fig. 1, 7] sandwiched between the active matrix substrate and the counter electrode substrate; the active-matrix substrate further including supplementary capacitance lines which

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are formed in parallel to the scanning electrode lines, and supplementary capacitances [Fig. 1, 8] for holding display data which are connected between the pixel electrodes and the supplementary capacitance lines, the apparatus further comprising: a supplementary capacitance drive circuit [Fig. 1, Ve] for driving the supplementary capacitance lines so that a predetermined potential difference between the voltage applied to the counter electrode and the voltage applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplementary capacitances leaks (see Column 6, Line 21 - Column 8, Line 50).

Moreover, Applicants' own admitted prior art discloses an active-matrix liquid crystal display apparatus [Fig. 7, 1] comprising: an active-matrix substrate [Fig. 7, 2] including a plurality of scanning electrode lines [Fig. 8, 11], a plurality of data electrode lines [Fig. 8, 12]. pixel electrodes [Fig. 8, 14] and switching elements [Fig. 8, 10], the pixel electrodes being respectively connected to intersections of the plurality of scanning electrode lines and the plurality of data electrode lines via the switching elements; a counter electrode substrate [Fig. 7. 3] including a counter electrode [Fig. 8, 16] formed thereon, the counter electrode being opposed to the pixel electrodes; a liquid crystal [Fig. 8, C_{LC}] sandwiched between the active matrix substrate and the counter electrode substrate; the active-matrix substrate further including supplementary capacitance lines [Fig. 8, 15] which are formed in parallel to the scanning electrode lines, and supplementary capacitances [Fig. 8, Cs] for holding display data which are connected between the pixel electrodes and the supplementary capacitance lines, the apparatus further comprising: a supplementary capacitance drive circuit [Fig. 8, Cs] for driving the supplementary capacitance lines so that a predetermined potential difference between the voltage applied to the counter electrode and the voltage applied to the pixel electrodes is always

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maintained [wherein, the amount that remains after Vcom is subtracted from Vcs is always equal to zero] when any of the pixel electrodes and supplementary capacitances leaks (see Figs. 7-9 and Pages 1-6).

However, neither aforementioned reference expressly discloses a supplementary capacitance drive circuit for driving the supplementary capacitance lines based on a voltage applied to the counter electrode so that a predetermined potential difference between the voltage applied to the counter electrode and a voltage applied to the pixel electrodes, which voltages are different from each other, is always maintained when any of the pixel electrodes and supplementary capacitances leaks. This distinct supplementary capacitance driving technique has been incorporated into all six independent claims (claims 1 and 19-23), thereby rendering them allowable.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

14 October 2004

BIPIN SHALWALA SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2600